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Analytical Modeling and Simulation of Advanced Silicon Nanowire Transistors

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Surrounding gate architecture for transistors has been shown to alleviate many of the problems posted by scaling and short channel effects. Semiconducting nanowires have recently attracted considerable attention in the semiconductor industry. With their unique electrical and optical properties, they offer interesting perspectives for basic research as well as for technology. In this paper, we have proposed a new analytical model for three different geometries of Surrounding Gate Silicon Nanowire Transistors. I–V characteristics (current-voltage) of the devices are effectively derived in all the three regions of operation. The variation of threshold voltage and drain current due to the device parameters like silicon thickness, doping concentration and radius are also predicted. Effectiveness of the models are fully validated by comparing the analytical results with the TCAD simulation results.

Keywords: Surrounding Gate Nanowire FETs, Rectangular Surrounding Gate Silicon Nanowire.

1. INTRODUCTION

In near future, it is possible that the Surrounding Gate Nanowire MOSFETs will find their own hold in integrated circuits field as these devices are bound to have certain advanced features which make them more compatible for the present-day semiconductor industry. Some of the advantages of these devices are the reduction in threshold voltage roll-off, DIBL and sub threshold swing. Hence, a number of research works are being carried out to characterize these devices, to understand their fabrication and simulation. Continuous scaling of nanowire MOSFETs results in the reduction of active silicon area of the device and it becomes essential

An analytical I-V model for SG transistors that includes quantum and velocity overshoot effects has been reported by Roldan et al [1]. It proposes a new analytical model for the inversion charge of Surrounding Gate transistors. Quantum effects are taken into account by means of a modified capacitance model that includes the inversion charge centroid and a correction to the threshold voltage. A drain current model for the SGT that includes velocity saturation, short channel and velocity overshoot effects is also developed. A unified short channel compact model for cylindrical surrounding gate MOSFET has been developed by Bastien et al., [2]. A continuous and explicit model that is valid for all operating regions of an undoped short channel cylindrical GAA transistor is presented. Short channel effects like DIBL and threshold voltage roll-off are explicitly modeled. These effects are then implemented into a drain current model based on an effective surface potential approach using the gradual channel approximation. Improving the model behavior in the saturation region by accounting for the channel pinch off displacement, channel length modulation is observed and implemented as well.

A compact drain current model for undoped cylindrical SG MOSFETs that includes the short channel effects has been proposed by Smaani [3]. The drain current model is expressed as a function of the mobile charge density, which is calculated using the analytical expressions of the surface potential and the difference between surface and centre potential models. The short channel effects are properly addressed in the drain current model and the results are validated by comparing with 3D numerical results.

A silicon nanowire FET compact model for circuit simulation has been developed by Jie Yang et al., [4]. Starting from the solution of Poisson's equation, an accurate inversion charge expression is derived for nanowire transistors with arbitrary body doping concentration. The drain current, transconductance, output conductance, terminal charges, and capacitances are then calculated based on fundamental device physics. The model is finally implemented in circuit simulators using Verilog-A, and its applications are also studied.

Modeling of silicon nanowire FETs based on their C-V and I-V characteristics has been done by Yoon-Ha Jeong et al [5]. From the C-V data, the effects of undoped floating channel on the silicon nanowire FET are analyzed. Mobility and intrinsic channel capacitance are extracted from the available data by eliminating the effects of parasitic capacitances. Also, the I-V data free from the effect of the series capacitance is obtained and combined with the compact model.

An analytical model of drain current in nanowire transistors that includes the quantum confinement, band structure effects and quasi ballistic transport has been presented by Dura et al., [6]. The architecture of the paper is aimed for ultra scaled devices up to technology nodes of sub-11nm and uses silicon films of a few nm in thickness.

A compact model for depletion mode p-type cylindrical surrounding gate nanowire MOSFET has been developed by YS.Yu and HK Park [7]. The model is proposed to have two back-to-back Schottky diodes for the metal-semiconductor contacts and the intrinsic nanowire FET. Based on the electrostatic method, the intrinsic nanowire FET model has been derived from current conduction mechanisms attributed to bulk charges through the central neutral region, in addition to accumulation charges through the surface accumulation region.

A simple analytical bulk current model for long channel double gate junctionless transistors has been proposed by Juan P.Duarte et al.,[8]. Using a depletion approximation, an analytical expression is derived from the Poisson equation to obtain the channel potential, which expresses the dependence of depletion width under an applied gate voltage. The depletion width equation is further simplified by the high channel doping concentration of the junctionless transistors. From the depletion width formula, the bulk current model is calculated using the ohm's law. And also, an analytical expression for subthreshold current is also derived.

A drain current model for triple gate n-type junctionless nanowire transistors has been developed by Trevisoli et al., [9]. The model is based on the solution of the Poisson equation. First, the 2-D Poisson equation is used to obtain the effective surface potential for long channel devices, which is used to calculate the charge density along the channel and the drain current. The solution of the 3-D Laplace equation is added to the 2-D model in order to take into account the short channel effects.

Many research works have been proposed to analytically derive the drain current of multi gate MOSFETs. But these above works have not addressed the exact impact created by the short channel effects on nanowire MOSFETS with ultra-short channels. Especially, there are very less drain current models available to understand the performance of Surrounding Gate Nanowire transistors. Hence, continuous and explicit drain current models for surrounding gate silicon nanowire transistors with three different geometries is proposed in this work. The models are based on the threshold voltage of the devices and are physically scalable with independent applied gate biases and oxide/channel thickness variations. Explicit regional solutions are derived for each analytical model and compared with each other to identify the device with optimum performance.

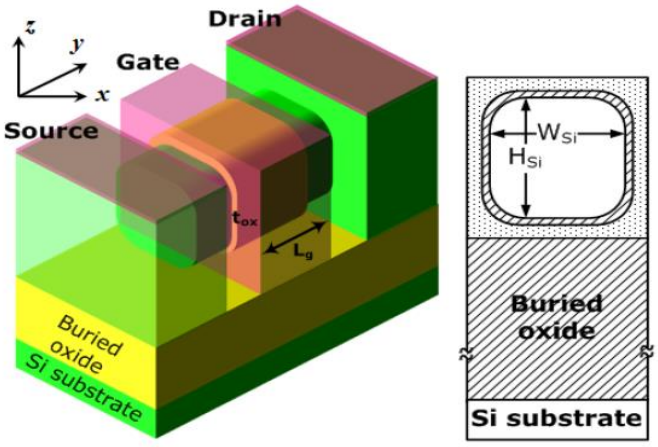
2. Analytical drain current modeling of rectangular SGNW transistors

In a Rectangular Surrounding Gate nanowire MOSFET, the drain current model is derived based on the closed form solutions of Poisson's and current continuity equations. The model has some distinct features implemented in its derivation.

1)The channel of the Rectangular SG nanowire MOSFET is assumed to be undoped, i.e., lightly doped instead of the usual high channel doping density. This feature helps in reducing the mobility degradation as it eliminates impurity scattering and random dopant fluctuations.

2)All three regions of operation are considered. The derived model is continuous and does not use any physical fitting parameters.

3)The model is based on the Pao-Sah integral without the charge sheet approximation. Hence the phenomenon of volume inversion in the subthreshold operation is predicted easily.



Figuer.1: Cross Sectional view of a Rectangular Surrounding Gate Silicon Nanowire Transistor

The Rectangular Surrounding Gate Nanowire can be considered as a device formed by combining two double gate devices. Hence the length of the channel is divided into two distinct

regions. Region L1 corresponds to the area of the channel under the influence of top and bottom gates while the region L2 indicates the region of the channel that is under the influence of the other two side gates. The hole density in the channel of the device is neglected and the Poisson equation of the Rectangular Surrounding Gate nanowire transistors is given by,

$$\frac{d^2\psi(x)}{dx^2} = \frac{d^2(\psi(x)-V)}{dx^2} = \frac{qn_i}{\varepsilon_{si}} e^{q\left(\frac{\psi(x)-V}{kT}\right)} \tag{1}$$

Where q is the electronic charge, n_i is the intrinsic carrier concentration, ε_{si} is the permittivity of silicon, $\Psi(x)$ is the silicon band bending, and V is the electron quasi-Fermi potential. In a Nanoscale device, the ballistic nature of the device is considered where the mean free path of the carriers is bigger than that of the silicon film width. Applying the gradual channel approximation, equation (1) is integrated to obtain the following equation.

$$\psi(x) = V - \frac{2kT}{q}\ln\left(\frac{t_{si}}{2\beta}\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}}\cos\frac{2\beta x}{t_{si}}\right) \tag{2}$$

The constant β is related to ψ through the boundary condition deduced from gauss's law.

$$\varepsilon_{ox}\frac{V_{gs}-\Delta\phi-\psi\left(x=\pm\frac{t_{si}}{2}\right)}{t_{ox}} = \pm\varepsilon_{si}\left.\frac{d\psi(x)}{dx}\right|_{x=\pm\frac{t_{si}}{2}} \tag{3}$$

Here ε_{ox} is the permittivity of oxide, V_{gs} is the voltage applied to gates, t_{si} and t_{ox} are the silicon and the effective oxide thicknesses, and $\Delta\phi$ is the work function of gate electrodes with respect to the intrinsic silicon. By substituting equation (2) into equation (3), we get a nonlinear equation relating β to various parameters of the device.

$$\frac{2\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta\tan\beta - \ln(\cos\beta) + \ln\beta = \frac{q\left(V_{gs}-\Delta\phi-V\right)}{2kT} - \ln\left(\frac{2}{t_{si}}\sqrt{\frac{2\varepsilon_{si}kT}{q^2 n_i}}\right) \tag{4}$$

The impact of the electrostatic potential is included in the total inversion charge of the device. The boundary condition for the device is now given as,

$$\frac{Q_{inv}}{\varepsilon_{si}} = 2\left.\frac{d\psi(x)}{dx}\right|_{x=\frac{t_{si}}{2}} \tag{5}$$

By using equation (2) and the boundary condition (5), the inversion charge is obtained as,

$$Q_{inv}(\beta) = \begin{cases} \dfrac{8\varepsilon_{si}}{t_{si}}\dfrac{kT}{q}\beta\tan\beta, 0 \le y \le L_1 \\ \dfrac{8\varepsilon_{si}}{t_{si}}\dfrac{kT}{q}\beta\tan\beta - 2qN_f, L_1 \le y \le L \end{cases} \tag{6}$$

The total reciprocal mobility in the device is assumed to be made of bulk mobility μ_o and oxide interface charge scattering mobility μ_{ox} and is given by,

$$\mu_i = \begin{cases} \mu_{o,}\ 0 \le y \le L_{1,} \\ \dfrac{\mu_o \mu_{ox}}{\mu_o + \mu_{ox}}, L_1 \le y \le L. \end{cases}$$

(7)

For a given V_{gs}, β can be solved from equation (4) as a function of V. As V varies from the source to the drain, the functional dependence of $V(y)$ and $\beta(y)$ is determined by the current continuity equation, which requires the current I_{ds} to be constant. The parameter μ is the effective mobility, and W is the device width. $dV/d\beta$ can also be expressed as a function of β by differentiating equation (4) to obtain,

$$\frac{dV}{d\beta} = -\frac{2kT}{q}\left[\frac{1}{\beta} + \tan\beta + 2\frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox} t_s i}\frac{d}{d\beta}(\beta \tan\beta)\right]. \tag{8}$$

The solution of Pao-Sah's integral can be found by integrating the continuity equation from the source to the drain and is given by,

$$I_{ds} = \mu_1 \frac{W}{L_1}\int_{o}^{V_p} Q_{inv}(V)dV = \mu_1 \frac{W}{L_1}\int_{\beta_s}^{\beta_p} Q_{inv}(\beta)\frac{dV}{d\beta}d\beta. \tag{9}$$

Applying the various factors in equation (9) and integrating,

$$I_{ds} = \mu_1 \frac{4W\varepsilon_{si}}{t_{si} L_1}\left(\frac{2kT}{q}\right)^2 \times \left[\beta\tan\beta - \frac{\beta^2}{2} + \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox} t_s i}(\beta\tan\beta)^2\right]_{\beta_p}^{\beta_s} \tag{10}$$

And for the region L_2 the current equation is given by,

$$I_{ds} = \mu_2 \frac{W}{L_d}\int_{V_p}^{V_{ds}} Q_{inv}(V)dV = \mu_2 \frac{W}{L_d}\int_{\beta_p}^{\beta_d} Q_{inv}(\beta)\frac{dV}{d\beta}d\beta. \tag{11}$$

Applying the various parameters as in previous case, equation (11) can be rewritten as follows.

$$I_{ds} = \mu_2 \frac{4W\varepsilon_{si}}{t_{si} L_d}\left(\frac{2kT}{q}\right)^2 \times \left[\beta\tan\beta - \frac{\beta^2}{2} + \frac{\varepsilon_{si} t_{oxeff}}{\varepsilon_{ox} t_{si}}(\beta\tan\beta)^2\right]_{\beta_d}^{\beta_p}.$$

$$-\mu_2 \frac{4WN_f kT}{L_d}\left[\ln\frac{\beta}{\cos\beta} + \frac{2\varepsilon_{si} t_{oxeff}}{\varepsilon_{ox} t_s i}(\beta\tan\beta)\right]_{\beta_d}^{\beta_p} \tag{12}$$

The drain current as a whole of the Rectangular SG device can be obtained by defining two functions that represent the right hand sides of equations (4) and (10).

$$f_r(\beta) = 2r\beta\tan\beta - \ln(\cos\beta) + \ln\beta \tag{13}$$

$$g_r(\beta) = \beta\tan\beta - \frac{\beta^2}{2} + r(\beta\tan\beta)^2 \tag{14}$$

The range of β is given as $0 < \beta < \pi/2$ and r is a structural parameter.

For the given values of V_{gs} and V_{ds}, β_s and β_d are calculated from the following conditions.

$$f_r(\beta_s) = (q/2kT)(V_{gs} - V_o) \tag{15}$$

$$f_r(\beta_d) = (q/2kT)(V_{gs} - V_o - V_{ds}) \tag{16}$$

$$V_o = \Delta\phi + \frac{2kT}{q}\ln\left(\frac{2}{t_{si}}\sqrt{\frac{2\varepsilon_{si}kT}{q^2 n_i}}\right) \tag{17}$$

Now the compact drain current model is finally given by,

$$I_{ds} = \mu_1 \frac{4W\varepsilon_{si}}{t_{si}L}\left(\frac{2kT}{q}\right)^2 \times \left[\beta\tan\beta - \frac{\beta^2}{2} + \frac{\varepsilon_{si}t_{oxeff}}{\varepsilon_{ox}t_{si}}(\beta\tan\beta)^2\right]_{\beta_d}^{\beta_s} \tag{18}$$

i) In the subthreshold region, the drain current is given by

$$I_{ds} = \mu_1 \frac{Wt_{si}n_i kT}{L_1} e^{\frac{q(V_{gs}-\Delta\phi)}{kT}}(1 - e^{\frac{-qV_p}{kT}}) + \mu_2 \frac{Wt_{si}n_i kT}{L_d} e^{\frac{q(V_{gs}-\Delta\phi)}{kT}}(1 - e^{\frac{-q(V_{ds}-V_p)}{kT}}) \tag{19}$$

ii) In the linear region above threshold, the drain current is given by

$$I_{ds} = 2\mu_1 C_{ox}\frac{W}{L_1}(V_{gs} - V_{th} - \frac{V_p}{2})V_p \tag{20}$$

iii) In the saturation region, the drain current is given by

$$I_{ds} = \mu_1 C_{ox}\frac{W}{L_1}\{(V_{gs} - V_{th})^2 - 2r(\frac{2kT}{q})^2 e^{\frac{q(V_{gs}-V_o-V_p)}{T}}\} \tag{21}$$

3. Analytical drain current modeling of rectangular SGNW transistors

The Junction Based Cylindrical Surrounding Gate Nanowire Transistor, considered to be an undoped or lightly doped device, is shown in Figure 6.2.

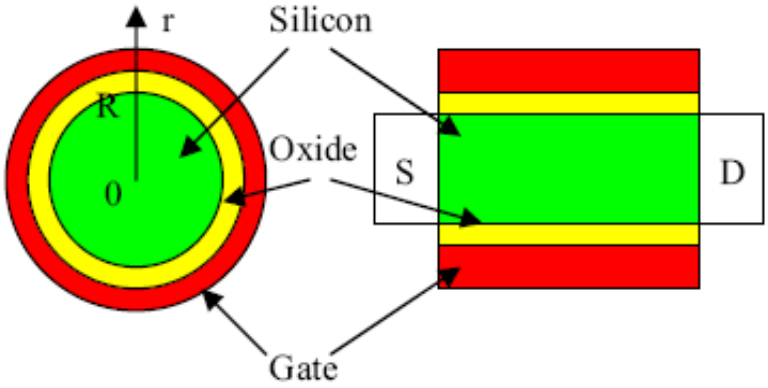


Figure. 2 :Cross Sectional view of a Junction Based Cylindrical Surrounding Gate Silicon Nanowire Transistor

Under gradual channel approximation, the Poisson's equation with only the mobile charges is given by,

$$\frac{\partial^2\phi}{\partial x^2}+\frac{1}{x}\frac{\partial\phi}{\partial x}=\frac{qn_i}{\varepsilon_{si}}e^{\frac{(\phi-V)}{v_T}} \tag{22}$$

Where q is the electronic charge, ε_{si} is the permittivity of silicon, n_i is the intrinsic carrier density, $\phi(x)$ is the electrostatic potential and V is the electron quasi-Fermi potential that is constant across the x direction. The hole density of the device is considered to be negligible and hence it is neglected.

The boundary conditions are

$$\frac{\partial\phi}{\partial x}\Big|_{x=0}=0 \tag{23}$$

$$\phi\big|_{r=R}=\phi_s \tag{24}$$

$$\frac{\partial^2\phi}{\partial x^2}=\frac{qn_i}{\varepsilon_{si}}e^{\frac{(\phi-V)}{v_T}} \tag{25}$$

Here ϕ_s is the surface potential at the radius R of the silicon nanowire and the equation (23) indicates that the electrical field is zero at the centre of the silicon body as a result of symmetry of the nanowire structure. The Channel potential is now represented by,

$$\phi(x)=V+v_T\ln[\frac{-8B}{\frac{q\eta}{\varepsilon_{si}}(1+Bx^2)}] \tag{26}$$

Where B is the constant related to the surface potential, v_T is the thermal voltage and η is the structural parameter used to obtain the potential.

$$\eta=\frac{4\varepsilon_{si}}{C_{ox}R} \tag{27}$$

i) In the linear region, the drain charge Q_D is dominant. Hence,

$$I_{ds} = 2\mu C_{ox}\frac{\pi R}{L}\left[V_{gs} - V_{th} - \frac{V_{ds}}{2}\right]V_{ds} \tag{28}$$

ii) In the saturation region, the device experiences a pinch off at the centre of the channel on the drain side and hence,

$$I_{ds} = \mu C_{ox}\frac{\pi R}{L}\left[\left(V_{gs} - V_{th}\right)^2 - V_{th}^{\,2}\left(\frac{\eta^2}{\left(1 - e^{\left(\frac{V_{gs} - V_{th} - V_{ds}}{v_T}\right)}\right)^2} + \frac{4\eta(1 - \eta/2)}{\left(1 - e^{\left(\frac{V_{gs} - V_{th} - V_{ds}}{v_T}\right)}\right)}\right)\right] \tag{29}$$

iii) In the subthreshold region the drain current is given by,

$$I_{ds} = \frac{\mu\pi R^2}{2} n_i kTe^{\left(\frac{V_{gs} - V_{th}}{v_T}\right)}\left[1 - e^{\left(\frac{-V_{ds}}{v_T}\right)}\right] \tag{30}$$

4. Analytical drain current modeling of junctionless cylindrical SGNW transistors

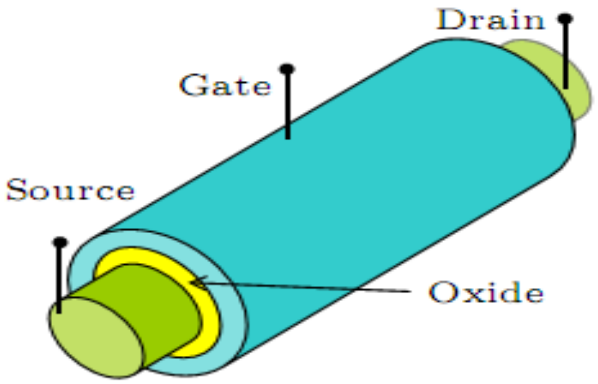


Figure.3 :Schematic view of a Junctionless Cylindrical Surrounding Gate Silicon Nanowire Transistor

Considering only mobile charges and Pao-Sah gradual channel approximation, the Poisson equation in the silicon region of Junctionless Cylindrical Surrounding Gate nanowire transistor is given by,

$$\frac{d^2\varphi(r,z)}{dz^2} = -\frac{qN_D}{\varepsilon_{si}}\left(1 - e^{\frac{(\varphi - V)}{v_T}}\right) \tag{31}$$

Where φ is the channel potential, ε_{si} is the permittivity of silicon, and V is the electron quasi Fermi potential. The total charge on the channel can be obtained by integrating the charge

density over the entire channel.

$$Q = qN_D t_{si} - qN_D \int_{-t_{si}}^{t_{si}} e^{\frac{(\varphi - V)}{v_T}} dz \tag{32}$$

The approach gives the following form of the Pao-Sah integral that includes the diffusion and drift current components.

$$I_{DS} = -\mu \frac{2\pi R}{L_{eff}} \int_0^{V_{ds}} Q_{mb} dv \tag{33}$$

i) In the linear region,

$$I_{DS} \cong \mu \frac{2\pi R \varepsilon_{ox}}{\beta L t_{ox}} \left(V_{gs} - V_{th} - \frac{V_{ds}}{2} \right) V_{ds} \tag{34}$$

ii) In the saturation region, the device experiences a pinch off at the centre of the channel on the drain side.

$$I_{DS} = -\mu \frac{2\pi R \varepsilon_{ox}}{\beta L t_{ox}} \left[\left(V_{gs} - V_{th} \right)^2 - \frac{\beta t_{ox}}{\varepsilon_{ox}} v_T \kappa \right] \tag{35}$$

$$\kappa = \sqrt{2\varepsilon_{si} \pi v_T q N_D} \times e^{\frac{\left(V_{gs} - V_{th} - V_{ds} \right)}{v_T}} \tag{36}$$

iii) In the subthreshold region,

$$I_{DS} \cong \mu \frac{2\pi R}{L} \left[v_T \sqrt{2\varepsilon_{si} \pi v_T q N_D} \times e^{\frac{\left(V_{gs} - V_{th} \right)}{v_T}} \psi \right] \tag{37}$$

$$\psi = \left(1 - e^{-\frac{\left(V_{ds} \right)}{v_T}} \right) \tag{38}$$

Thus the drain current model of a Junctionless cylindrical Surrounding Gate Silicon Nanowire transistor is obtained for all three operating regions of the device.

5. Results and discussion

Figure 4 shows the relationship between the drain current and drain to source voltages of a Rectangular Surrounding Gate Nanowire transistor. The plot deduces the relationship for different values of gate to source voltages of the device. There is a gradual increase in the drain current with the increase in gate to source voltage. A maximum drain current 0.45 microamperes is obtained for the value of Vgs=1.5V. This explains the impact of gate voltage on the performance of the device. A comparison between the analytical model and simulation data obtained using TCAD has also been performed with a good agreement.

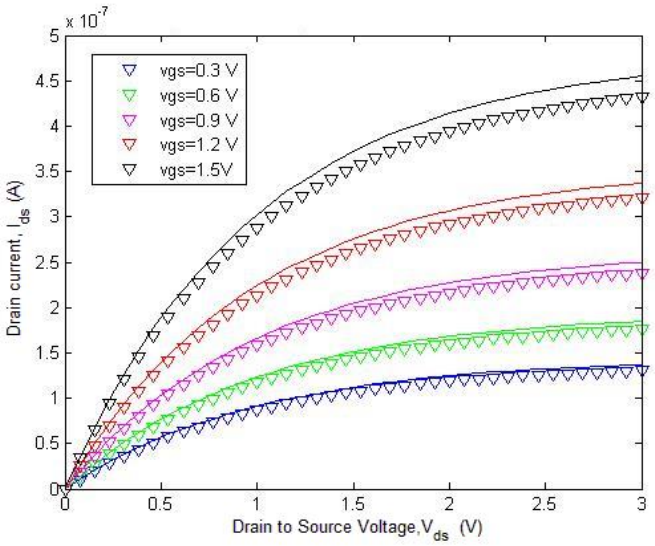
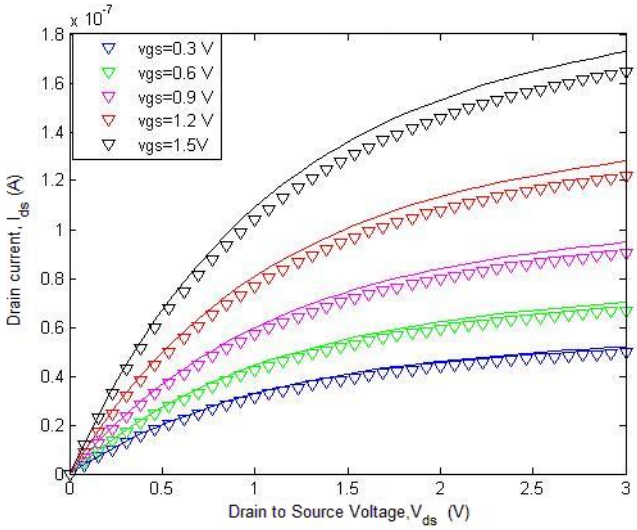


Figure.4 : Drain current versus Drain to Source Voltage Plot for different Gate to Source voltages of a Rectangular Surrounding Gate Naowire Transistor

Figure 5 shows the relationship between the drain current and drain to source voltages of a Junction Based Cylindrical Surrounding Gate Nanowire transistor. The plot shows the relationship as a function of different gate to source voltages of the device. There is a gradual increase in the drain current with the increase in gate to source voltage. A maximum drain current 0.17 microamperes is obtained for the value of Vgs=1.5V. This explains the impact of gate voltage on the performance of the device. A comparison between the analytical model and simulation data obtained using TCAD has also been performed with a good agreement.



Junction **Figure.5 :** Drain current versus Drain to Source Voltage Plot for different Gate to Source voltages of a Based Cylindrical Surrounding Gate Nanowire Transistor

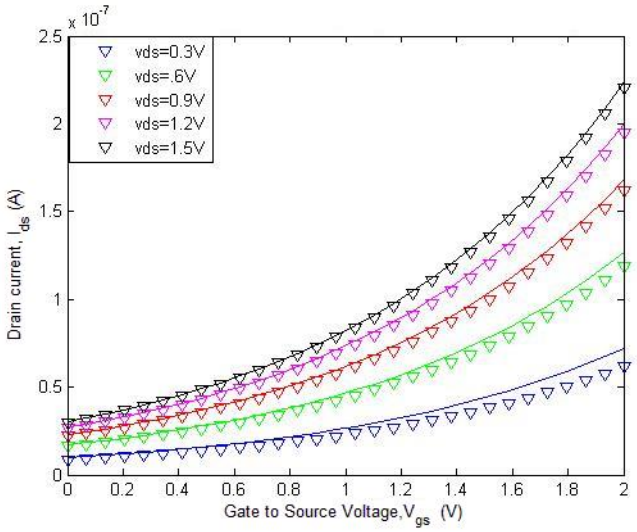


Figure.6 :Drain current versus Gate to Source Voltage Plot for different Drain to Source voltages of a Junction Based Cylindrical Surrounding Gate Nanowire Transistor

Figure 6 shows the relationship between the drain current and gate to source voltages of a Junction Based Cylindrical Surrounding Gate Nanowire transistor. The plot deduces the relationship for different values of drain to source voltages of the device. A maximum drain current of 0.22 microamperes is observed for the value of Vds=1.5V. Good correlation between the analytical model and simulation results validate the proposed model. The analytical model continuously predicts the characteristics of a Junction Based Cylindrical SG Nanowire transistor in all three regions of operation.

Figure 7 shows the relationship between the drain current and gate to source voltages of a Junctionless Cylindrical SG Nanowire transistor. The transfer characteristics of the device are plotted as a function of different drain to source voltages. It shows that the drain current increases nonlinearly with gate to source voltage for different Vds of 0.3V, 0.6V, 0.9V, 1.2V and 1,5V. A maximum drain current of 0.4 microamperes is observed for the value of Vds=1.5V. From this figure, it can be noted that the analytical model is in clear agreement with the TCAD simulation results.

Thus the drain current characteristics of all three geometries of Surrounding Gate Silicon Nanowire Transistors have been studied. Now, in order to identify the device that gives the optimum performance for semiconductor technology, we are in need of comparing the characteristics of these three devices.

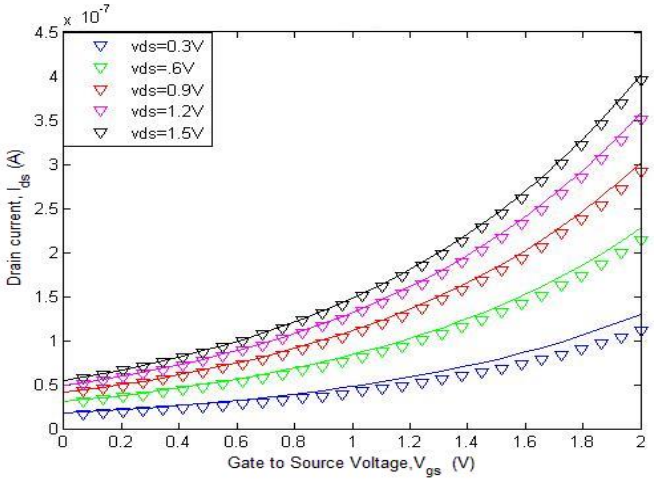


Figure.7 :Drain current versus Gate to Source Voltage Plot for different Drain to Source voltages of a Junctionless Cylindrical Surrounding Gate Nanowire Transistor

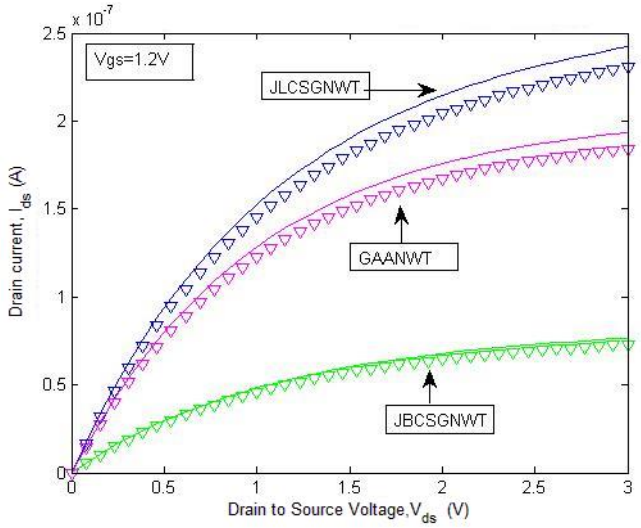


Figure.8 :Drain current versus Drain to Source Voltage Plot for three different geomtries of Surrounding Gate Nanowire Transistors

A plot that compares the drain current characteristics of all three geometries of Surrounding Gate nanowire transistors studied in this dissertation has been shown in Figure 8. The effective length of the channel is presumed to be the same for all three devices at Leff=10nm. The gate bias is maintained constant at 1.2 V and the drain to source voltages are varied. The relatively large on-state current shows that the Junctionless device has a clear edge over the other two geometries. This can be attributed to the fact that the device has an excellent subthreshold swing due to the fixed voltage drop along the silicon wire and the oxide under complete depletion of the channel.

A plot that compares the drain current characteristics of all three geometries of Surrounding Gate nanowire transistors studied in this dissertation has been shown in Figure 9. The effective length of the channel is presumed to be the same for all three devices at Leff=30nm. The drain bias is maintained constant at 2 V and the gate to source voltages are varied. The relatively large drain current of the Junctionless device proves that it has a superior performance in comparison with the other two geometries.

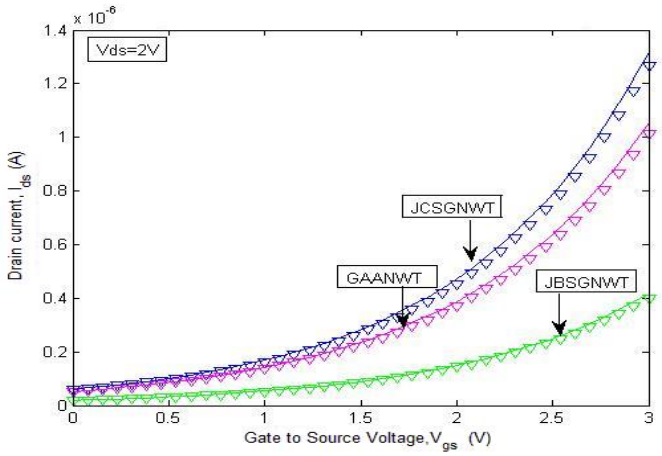


Figure.9 :Drain current versus Gate to Source Voltage Plot for three different geometries of Surrounding Gate Nanowire Transistors

6. Conclusion

In this work, the analytical drain current models for three different geometries of Surrounding Gate Silicon Nanowire Transistor are derived and compared to obtain the device with the optimum performance. The analytical models are derived using the Pao-Sah integral and gradual channel approximation. Performance of devices in all three regions of operation is determined. The model clearly predicts the impact of gate bias, drain bias and the doping concentration on the drain current characteristics of all three geometries. A simple comparison between the transfer characteristics of the device explains the superiority of the Junctionless device over other two geometries. The analytical models are validated by comparing the results with the simulations of numerical simulator Sentaurus TCAD.

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